IEEE International Solid-State Circuits Conference

Sunday -Thursday, February 11 - 15, 2007
San Francisco Marriott Hotel, San Francisco, CA

Innovative and original papers are solicited in subject areas including (but not limited to) the following:

ANALOG& RF —- amplifiers; dc-dc converters; continuous-time & discrete-time filters; comparators; multipliers; voltage references; power-control circuits; consumer electronics; non-linear analog circuits, op amps, switched-capacitor circuits. Note that now we also consider circuits and subcircuits for RF/IF/baseband including: receiver and transmitter front-end circuits, IF amplifiers, power amplifiers, RF switches, power detectors, active antennas, modulators, demodulators, phase-locked loops, frequency synthesizers.

DATA CONVERTERS — Nyquist-rate and oversampling A/D and D/A converters; sample-and-hold circuits.

DIGITAL —- design, fabrication, and test of digital VLSI systems; microprocessors and network processors; I/O and inter-chip communication; digital-noise isolation techniques; intra-chip communication; reconfigurable logic arrays; clock-synthesis circuits and architectures; high-performance and low-power logic-micro-architectures and circuit techniques; high-speed digital circuits, power reduction and management methods for digital VLSI.

IMAGERS, MEMS, MEDICAL & DISPLAY —- image sensors and companion chips; smart sensors; MEMS for analog and RF; MEMS for sensor-and-instrumentation applications, integrated sensors and transducers; sensor-interface circuits; biosensors; microarrays and lab-on-a-chip; sensors for medical applications; circuitry and MEMS technologies that enable bio-medical and environmental applications; display drivers, controllers, and companion chips; thin-film-transistor interface circuits; organic LED and liquid-crystal-display interface circuits; flat-panel and projection displays; circuits for print heads.

MEMORY —- static, dynamic, non-volatile, and read-only memory; circuit-design techniques, system architectures, I/O interfaces, and array organizations; magnetic and ferro-electric memory designs and architectures; data storage and multi-bit-cell-based memory designs; embedded memory architectures, cache-memory systems, multi-port memory, and CAM designs; emerging memory technologies: nano-crystal, phase-change, and 3D memories; high-speed low-power and low-voltage memory designs; yield-enhancement redundancy, and ECC techniques; memory testing and built-in self-test.

SIGNAL PROCESSING -– digital signal processors; reconfigurable signal-processing circuits; low-power signal-processing circuits; baseband communication processing architectures; cryptographic and security processing circuits; analog signal-processing circuits; magnetic and optical-storage circuits; multimedia processors, image processing/compression architectures; audio-and-voice- processing/compression architectures, graphics processors.

TECHNOLOGY DIRECTIONS —- advanced circuit technologies and techniques; ultra-low-voltage mixed-signal circuit techniques; molecular-, organic-, and nano-electronics; flexible substrates, and printable electronics; 3D-integration and novel packaging technologies; compound-semiconductor, superconductive, and micro-photonic technologies and circuits; energy sources, and energy harvesting; emerging applications such as bio-medical, ambient-intelligence, and wearable-electronics; emerging wireless applications and circuits, such as ultra-low-power and ultra-wideband, 3D RF technology; RFID; advanced signal-processing and microprocessor architectures; analog and optical processors, non-transistor-based analog and digital circuits and their system architectures; advanced memory technologies; and quantum storage.

WIRELESS —- receivers/transmitters/transceivers for wireless systems including (but not limited to) Bluetooth, WLAN, WPAN, WMAN, GPS, UWB, GSM/EDGE/CDMA/UMTS/3G base stations and handsets, TV/radio/satellite, DVB/DMB, MMDS.

WIRELINE —- receivers/transmitters/transceivers for wireline systems including (but not limited to) LAN, WAN, FDDI, Ethernet, token ring, fiber channel, SONET, SDH, PON, ATM, ISDN, xDSL, cable-modem; optical/electrical data links and backplane transceivers, power-line/phone-line home networks, subscriber-line circuits and modems. Wireline transceiver building blocks like AGC, amplifiers, oscillators, phase-locked loops, line-drivers and hybrids.

A submission may be accepted as either a regular paper or a short paper. A regular paper is allowed 23 minutes for presentation and 7 minutes for questions. Short papers are allowed 15 minutes total for both presentation and questions. Regular and short papers have the same submission requirements and quality standards. They differ only in the determination by the Program Committee of the time required to present their key ideas. Companion papers for large chips, ones that require two paper slots to discuss both architecture and circuit details, are encouraged (identify companion papers during the submission). Please refer to the sample Abstract on the ISSCC Web site (www.isscc.org/isscc).

• 2007 Conference Theme •

"The 4 Dimensions of IC Innovation"

Submission Deadline is Friday, September 15, 2006
3:00PM Eastern Standard Time (19:00 GMT)